QUESTION BANK 2017



## SIDDHARTH GROUP OF INSTITUTIONS :: PUTTUR Siddharth Nagar, Narayanavanam Road – 517583 <u>QUESTION BANK (DESCRIPTIVE)</u>

Subject with Code : ALFVLSI (16EC5710) Year & Sem: I-M.Tech & II-Sem **Branch & Specialization**: M.Tech – VLSI **Regulation**: R16

## <u>UNIT –I</u> <u>PRELIMINARIES</u> GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION

	GENERAL I UNI USE METHODS FOR COMBINATIONAL OF HIMILATION	
1.	(a)What are the most important entities in VLSI design and explain in detail?	[5M]
	(b)Draw the decomposition tree and explain.	[7M]
2.	(a)How combinational optimization is achieved using Local and Tabu search?	[6M]
	(b)Explain the following: (i) Backtracking. (ii) Branch and bound programming	[6M]
3.	(a) Explain the different design automation tools for VLSI design	[6M]
	(b)Explain algorithms for constrained graph compaction	[6M]
4.	Explain about the design methodology based on top-down structural decomposition and b	oottom
	up Layout reconstruction using Gajski's y-chart.	[12M]
5.	What are the several purpose methods for combinational optimization? Explain briefly.	[12M]
6.	(a)What is the importance of design automation tools.	[3M]
	(b) Describe any three design automation tools	[9M]
7.	(a)Analyze what is the need of genetic algorithm.	[6M]
	(b)Explain about Genetic Algorithms.	[6M]
8.	Write about the combinatorial optimization problems and decision problems.	[12M]
9.	Design dynamic programming approach for travelling salesman problem	[12M]
10	With example explain briefly tractable and intractable problems related to VLSI design	
	automation	[12M]

# UNIT-II LAYOUT COMPACTION MODELLING AND SIMULATION

1.	Explain briefly the following:	
	(a)The concept of placement in VLSI design.	[6M]
	(b)The routing problems and routing techniques in VLSI design.	[6M]
2.	(a)With an example, explain the difference between modeling and simulation.	[6M]
	(b)Perform Gate level and switch level modeling for parallel codes.	[6M]
3.	(a)What is floor planning?	[6M]
	(b) Compare the compiler driven simulation and event driven simulation	[6M]
4.	(a)What is layout compaction? Explain algorithms for constrained graph compaction	[6M]
	(b) Explain about the important abstraction levels that are necessary for a specific simula	ation tool.
		[6M]
5.	(a) What is the placement? What is the requirement of placement?	[5M]
	(b) Explain the concept of placement with respect to layout synthesis.	[7M]
6.	What is meant by modeling and simulation? Differentiate gate level and switch level	modeling
	and simulation procedures with suitable example	[12M]
7.	(a)What is the concept of layout compaction and clearly explain how compaction is usef	ul for
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 VLSI design?
 [6M]

 (b)Explain with an algorithm how routing problems can be overcome?
 [6M]

 8. (a)Summarize the important abstraction levels that are necessary for a specific simulation tool
 [6M]

 (b)Discuss about the compiler driven simulation and event driven simulation.
 [6M]

 9. With suitable examples explain the switch level modeling and simulation
 [12M]

 10. Explain the routing problems in floor planning methods of VLSI design.
 [12M]

### UNIT III LOGIC SYNTHESIS AND VERIFICATION

1	(a) Draw Binary-Decision diagrams for an Inverter	[6M]
1.	(a) Draw Dinary-Decision diagrams for an inverter	[6M]
~	(b) write short notes of logic synthesis	
2.	(a) What are the principles of reduced ordered binary decision diagram?	[6M]
	(b)What are the issues and terminology involved in the combinational logic synthesis	
		[6M]
3.	(a)Explain ROBDD implementation and construction	[6M]
	(b)With example explain the ROBDD manipulation?	[6M]
4.	Explain Heauristic based on ROBDD?	[12M]
5.	(a) What is the principle of ROBDD?	[4M]
	(b) Explain how OBDD size is reduced to obtain ROBDD?	[4M]
	(c) Explain how ROBDDS can be used for logic verifications?	[4M]
6.	(a) What is a combinational logic synthesis?	[6M]
	(b) With practical example explain the combinational logic synthesis?	[6M]
7.	Explain the following	
	(a)ROBDD principles	[6M]
	(b)ROBDD implementation and construction	[6M]
8.	Explain the following related to ROBDD	
	(a) Variable ordering	[6M]
	(b) Applications to verification	[6M]
9.	Explain how ROBDD can be used for combitorial optimization	[12M]
10	. (a) What is two level logic synthesis	[4M]
	(b)Explain problem definition and analysis in two level logic synthesis	[8M]

#### <u>UNIT –IV</u> HIGH-LEVEL SYNTHESIS

1.	(a) List & explain any two scheduling algorithms.	[6M]
	(b) Describe High-level Transformation	[6M]
2.	(a) Explain the Force-directed scheduling in detail.	[6M]
	(b)Write about the Hardware models for High-level synthesis.	[6M]
3.	(a) What is the internal representation of the input algorithm?	[4M]
	(b)Explain any three methods	[8M]
4.	Explain the following algorithms	
	(a) ASAP algorithm.	[6M]
	(b) Mobility based scheduling.	[6M]

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5. (a)What type of Hardware components can be used by a high level synthesis system?       [6M]         (b) Explain how the ASAP scheduling algorithm is used to find the longest path?       [6M]         6. With detailed example explain the allocation, assignment and scheduling       [12M]         7. Explain the following algorithms       [6M]         (a) Force directed scheduling       [6M]         (b) List scheduling       [6M]         8. What are the aspects of assignment problem? Explain.       [12M]         9. (a)Explain the high level transformations.       [6M]         (b) Explain the following algorithms       [6M]         (a) Simple dataflow       [4M]         (b) Conditional dataflow       [4M]         (c) Iterative dataflow       [4M]         (c) Iterative dataflow       [4M]         (c) Iterative dataflow       [4M]         (c) Iterative dataflow       [6M]         (b) How partitioning is performed for staggered model       [6M]         (b) Programmable MCM's       [6M]         (a) Explain the types of logic blocks for FPGA with neat sketches       [6M]         (b)Drogrammable MCM's       [6M]         (a) Explain the types of logic blocks for FPGA with neat sketches       [6M]         (b)Drogrammable MCM's       [6M]         (a) Write shain the foll		QUESTION BANK	2017
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<ul> <li>4. (a) With neat sketch explain about the physical design cycle of MCM. [6M]</li> <li>(b)Briefly explain about the different approaches to be followed for General MCM routing problems. [6M]</li> <li>(a) Explain the FPGA technologies. [6M]</li> <li>(b) How partitioning is performed for segmented model [6M]</li> <li>(a) Briefly explain MCM technologies. [6M]</li> <li>(b) What are the different methods of MCM routing? Explain. [6M]</li> <li>7. Explain the types of logic blocks and routing models for FPGA with neat sketches [12M]</li> <li>8. Explain the following routing algorithms <ul> <li>(a) Topological routing</li> <li>(b) Integrated pin distribution and routing</li> <li>(c) How the routing network is modeled in FPGA? [6M]</li> <li>(d) How the routing Algorithm for staggered model and compare it with segmentation model. [6M]</li> </ul> </li> <li>10. (a) What are the various steps in MCM physical design cycle? Explain them briefly. [6M]</li> </ul>		(b)Develop a routing algorithm for the Non-segmented model.	[6M]
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Prepared by: <u>N.REVATHI</u>